Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming a storage node contact of a semiconductor device, the method comprising~~ the steps of~~:

depositing sequentially a conductive layer, a nitride layer and a polysilicon layer ~~on~~ over a substrate, where ~~having an insulating structure and a conductive structure~~at least one contact plug contacts the substrate;

~~etching selectively the~~ patterning the polysilicon layer, the nitride layer and the conductive layer to form ~~a plurality of conductive patterns~~ at least first and second conductive patterns, the patterned conductive layer defining the first and second conductive patterns, the patterned polysilicon and nitride layers defining ~~with a stack structure of the conductive layer and a~~ first and second dual hard mask patterns provided over the first and second patterned conductive patterns, respectively, wherein the first and second conductive patterns define a first hole therebetween, the first hole being provided directly over the contact plug ~~including the polysilicon layer and the nitride layer~~;

forming an insulation layer over the first and second dual-hard masks and into the first hole~~along a profile containing the conductive patterns~~; and

selectively etching the insulation layer to define a second hole and expose the contact plug~~by using a line type photoresist pattern as an etch mask to form a contact hole exposing the conductive structure disposed between the neighboring conductive patterns.~~

2. (Currently Amended) The method as recited in claim 1, the method further including: ~~after the step of forming the contact hole, further including the steps of:~~

after forming the second hole, depositing an oxide layer at least along a profile ~~containing~~ of the ~~contact~~ second hole; and

thereafter, forming a spacer at sidewalls of each conductive pattern by etching the oxide layer through a blanket etch-back process.

3. (Original) The method as recited in claim 1, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the bitline patterns are formed.

4. (Original) The method as recited in claim 1, wherein the nitride layer has a thickness ranging from about 900 Å to about 1500 Å.

5. (Currently Amended) The method as recited in claim 1, wherein the first and second conductive patterns are ~~is one of a~~ bit lines, ~~a~~ gate electrodes, or ~~and a~~ metal wire.

6. (Original) The method as recited in claim 1, wherein the conductive layer is made of a material selected from a group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

7. (Original) The method as recited in claim 1, wherein the plug is formed with one of polysilicon and titanium nitride.

8. (Original) The method as recited in claim 1, the insulation layer is made of a material selected from a group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass (SOG).

9. (Currently Amended) The method as recited in claim 1, wherein the insulation layer is etched using a line type photoresist pattern as an etch mask to define the second hole exposing the contact plug, wherein ~~further comprising the steps of removing~~ the photoresist pattern is removed after ~~the step of~~ forming the ~~contact~~ second hole.

10. (Currently Amended) The method as recited in claim ~~1~~9, wherein ~~at the step of forming~~ the photoresist pattern is formed ~~, photolithography~~ using a light source of ArF or KrF ~~is used to form the photoresist pattern~~.

11. (Currently Amended) The method as recited in claim 1, further comprising ~~the steps of~~:

providing conductive material over the polysilicon layer, the conductive material filling the second hole; ~~depositing a plug material into the contact hole so that the plug material is contacted to the exposed conductive structure;~~ and

removing the at least ~~plug~~ conductive material~~, the insulation layer~~ and the polysilicon layer to form a planarized conductive structure that electrically couples to the contact plug, the conductive structure having an upper surface that is substantially planar to an upper surface of the nitride layer~~in a manner of exposing the nitride layer to form a plurality of plugs planarized at the same surface level of the exposed nitride layer~~.

12. (Currently Amended) A method for fabricating a semiconductor device, the method comprising~~ the steps of~~:

depositing sequentially a bit line conductive layer, a nitride layer and a polysilicon layer ~~on~~ over a substrate in which a first plug is formed;

etching ~~selectively~~ the polysilicon layer, the nitride layer and the bit line conductive layer to form at least first and second ~~a plurality of~~ bit lines, the etched polysilicon and nitride layers defining first and second dual-structure mask patterns provided over the first and second bit lines, respectively ~~s with a stack structure including the conductive layer and a hard mask with a dual structure of the polysilicon layer and the nitride layer~~;

forming an insulation layer ~~along a profile containing the bit lines~~ over the first and second dual-structure mask patterns and into a first hole defined between the first and second bit lines, the first hole being defined directly over the first plug; and

etching the insulation layer ~~by using a line type photoresist pattern as an etch mask~~ to form a ~~contact~~ second hole exposing the first plug~~ disposed between the bit lines~~.

13. (Currently Amended) The method as recited in claim 12, the method further including~~after the step of forming the contact hole, further including the steps of~~:

after forming the second hole, depositing an oxide layer at least along a profile of ~~containing~~ the ~~contact~~ second hole; and

thereafter, forming a sidewall spacer ~~at sidewalls of~~ for each bit line by etching the oxide layer through a blanket etch-back process.

14. (Original) The method as recited in claim 12, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the bit lines are formed.

15. (Original) The method as recited in claim 12, wherein the nitride layer has a thickness ranging from about 900 Å to about 1500 Å.

16. (Original) The method as recited in claim 12, wherein the conductive layer is made of a material selected from a group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

17. (Original) The method as recited in claim 12, the insulation layer is made of a material selected from a group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass (SOG).

18. (Currently Amended) The method as recited in claim 12, further comprising ~~the steps of~~:

depositing a plug material into the ~~contact~~ second hole and over the ~~so that the plug material is contacted to~~ the exposed first plug; and

removing at least the plug material~~,~~ ~~the insulation layer~~ and the polysilicon layer to form at least one second plug that electrically couples the first plug,

wherein the plug material and the polysilicon layer are removed until ~~in a manner of exposing~~an upper surface of the nitride layer and is substantially planar to an upper surface of the second plug. ~~to form a plurality of second plugs planarized at the same surface level of the exposed nitride layer.~~